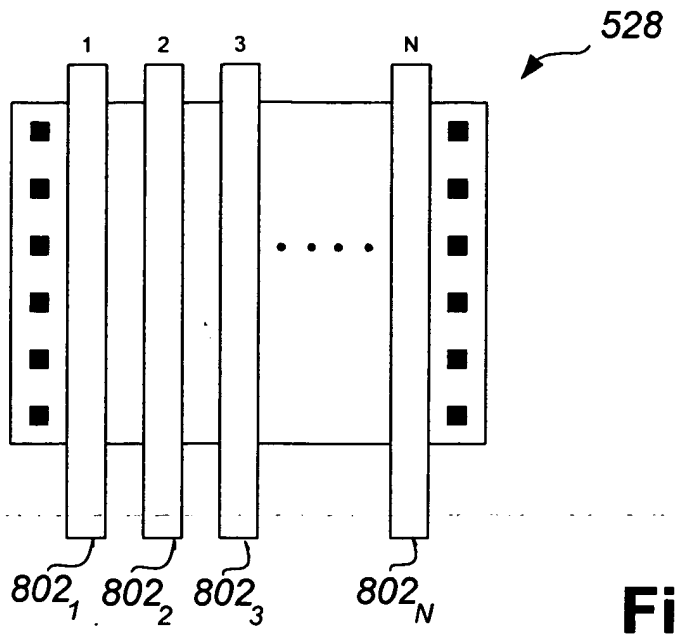
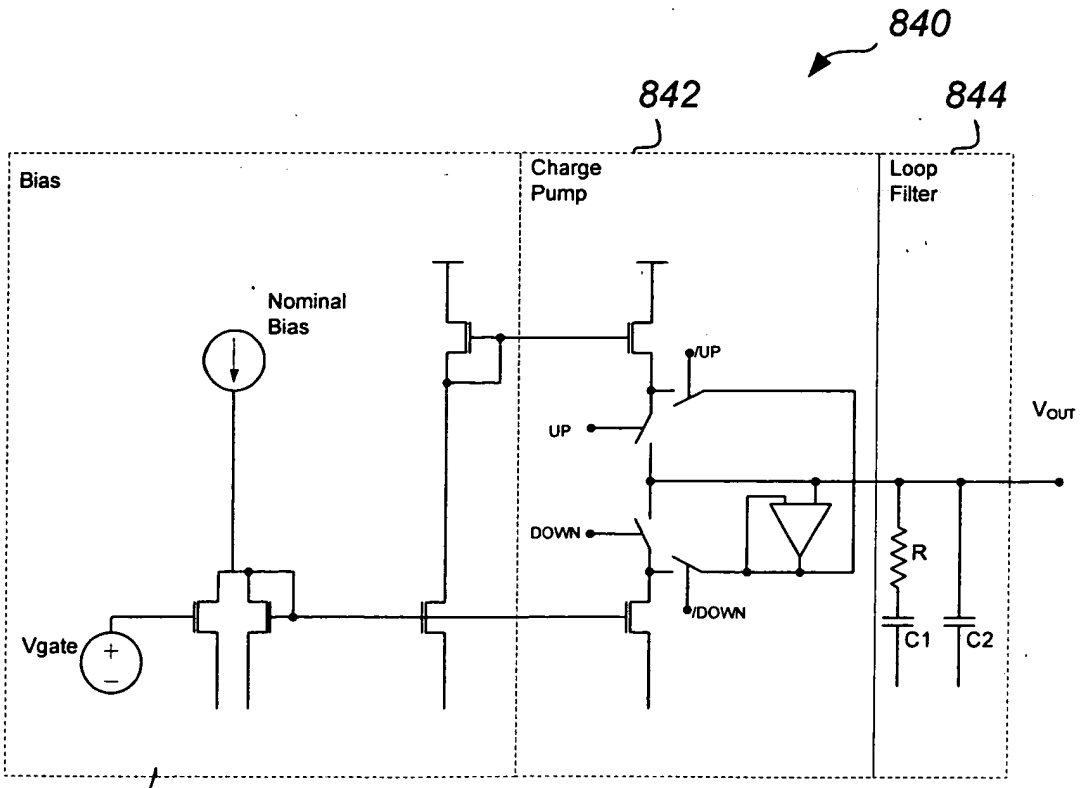


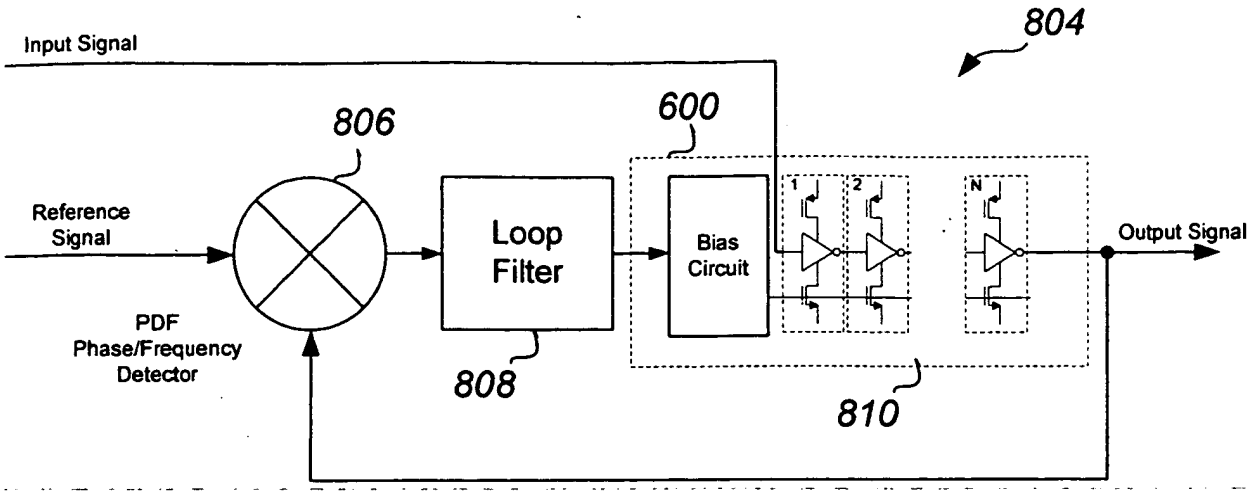
Plurality of Stripes

Fig. 19



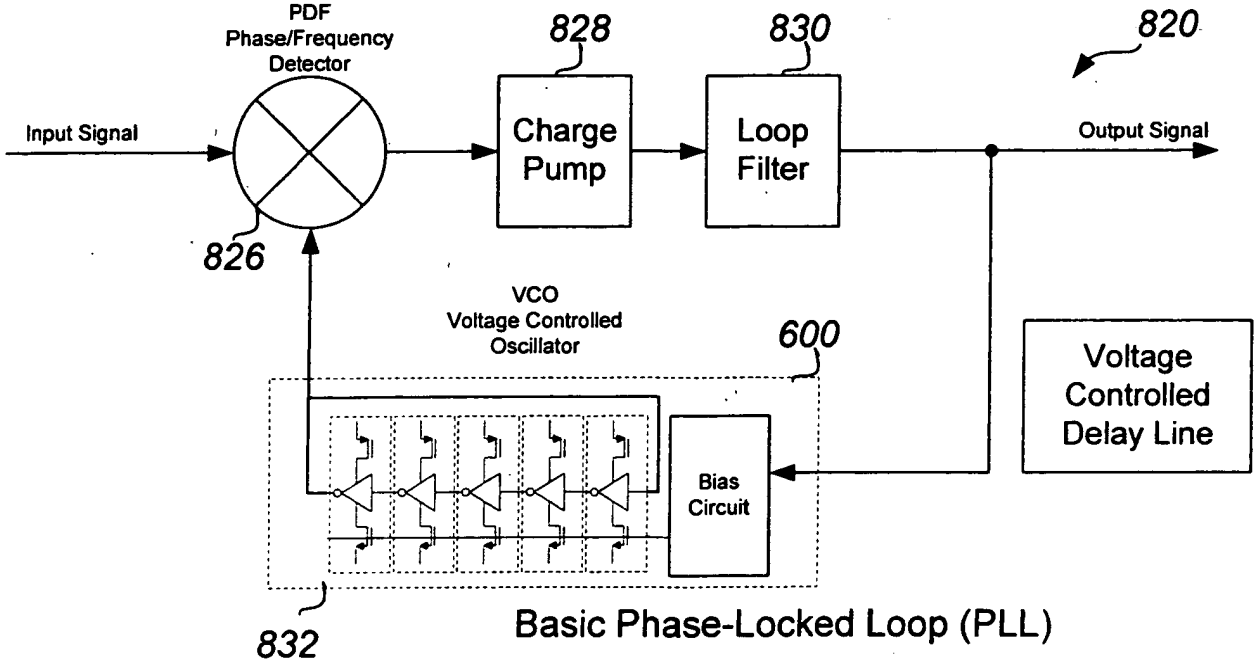
600 Charge Pump with Bias

Fig. 22



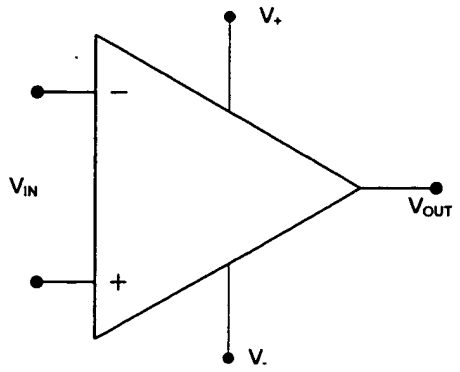
Basic Delay-Locked Loop (DLL)

Fig. 20



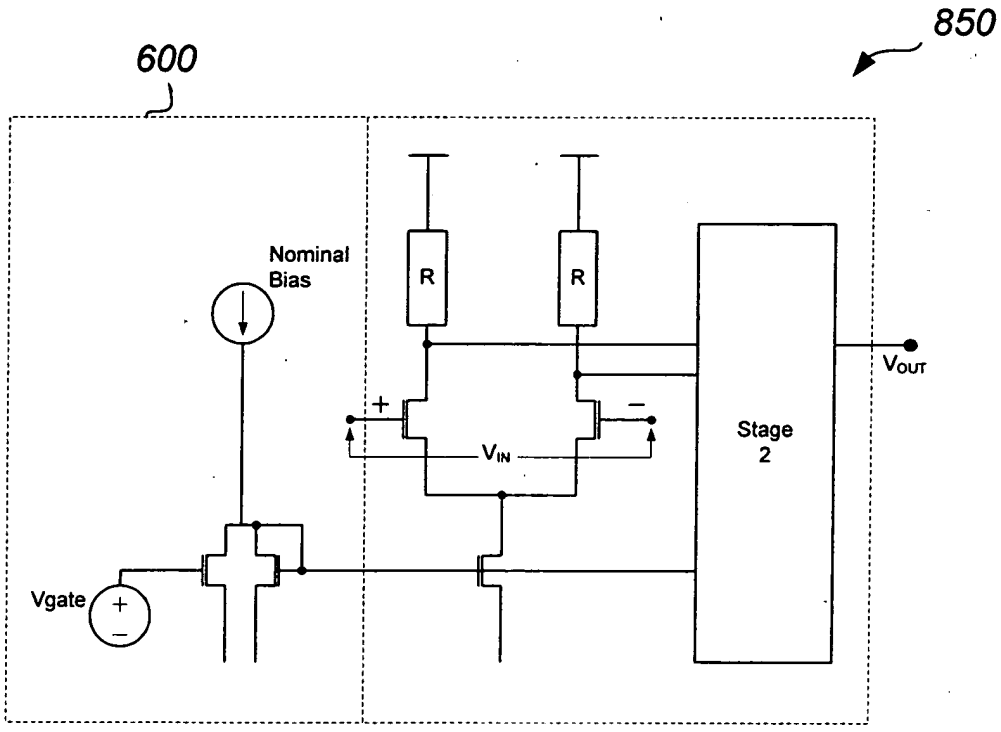
Basic Phase-Locked Loop (PLL)

Fig. 21



Operational Amplifier

Fig. 23a



Operational Amplifier with Bias Control

Fig. 23b

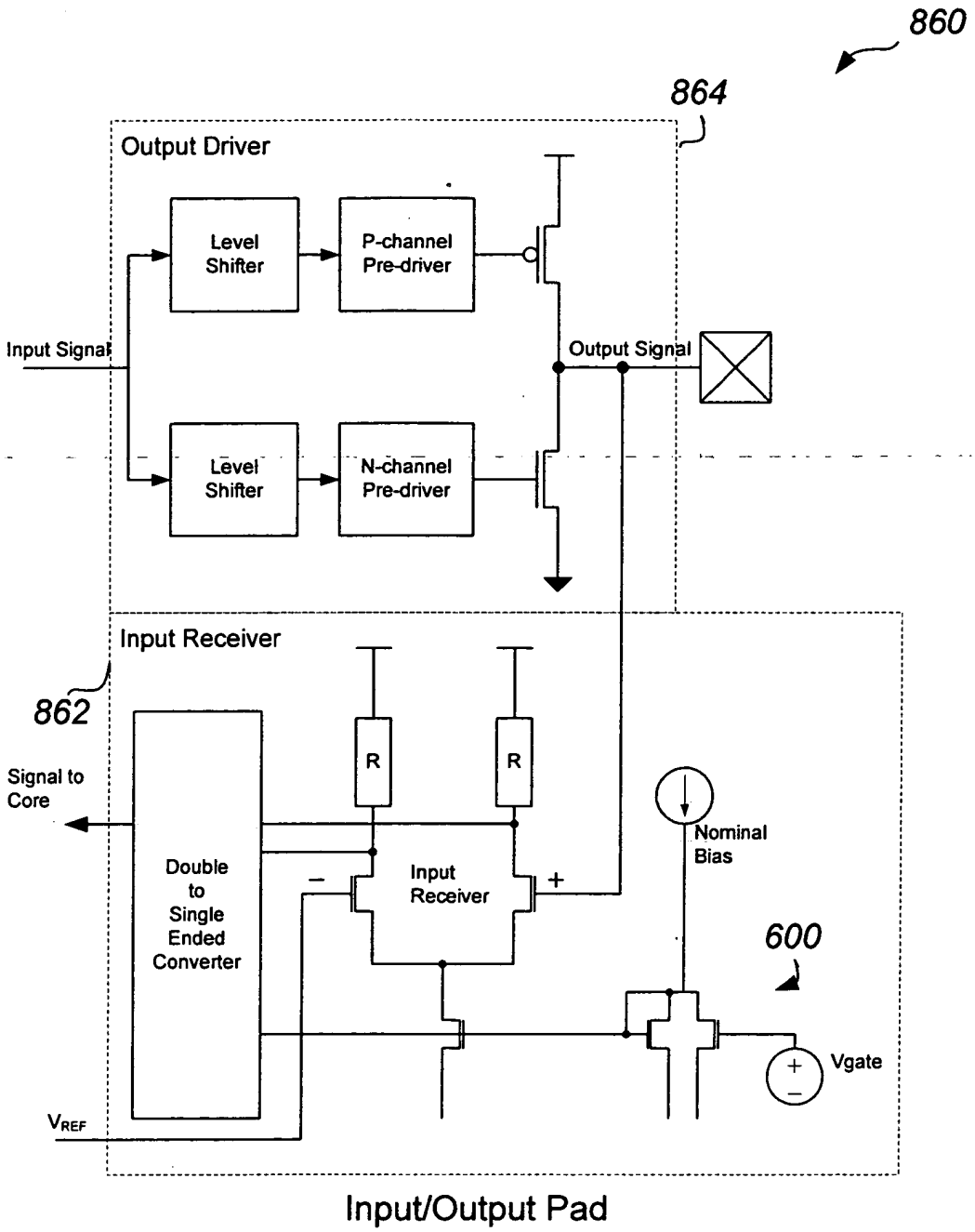

860
864
Output Driver
Level Shifter
P-channel Pre-driver
Input Signal
Output Signal
Level Shifter
N-channel Pre-driver
Input Receiver
862
Signal to Core
R
R
Nominal Bias
Double to Single Ended Converter
Input Receiver
600
Vgate
VREF
Input/Output Pad

Fig. 24